



V Rose Microsystems, Inc.

www.vrosemicrosystems.com

VRM-AMC-3C87F

Product Data Sheet

Overview:

The **VRM-AMC-3C87F** is a single width, full-size Advanced Mezzanine Card with exceptional processing performance and bandwidth, for the latest wireless baseband applications. A total of nine 1GHz DSP cores and a Xilinx Virtex-5 SX95T FPGA allow an application to be partitioned and optimised for most effective use of system resources. High bandwidth optical interfaces can be installed in the dual SFP sockets, providing an optical CPRI/OBSAI antenna interface or other options including an optical Ethernet backhaul or Serial RapidIO. Linked to these interfaces is a highly flexible, low jitter programmable PLL circuit, allowing a wide range of wireless synchronisation options including a low cost 1 PPS GPS clock. A range of build options are available, and further customisation is possible in volume, to enable the best technical and commercial fit to a customer application to be achieved.



Features:

HARDWARE SPECIFICATIONS

FPGA: Xilinx Virtex-5™ FPGA. Standard configuration is SX95T-2, options include LX110T, LX155T, FX100T. With:

- 2 independent banks of 128Mbytes x16 DDR2-600 SDRAM
- 128Mbytes of parallel FLASH
- 10Gbps 4x SRIO

• 2 Full-duplex Gigabit Ethernet ports
• 4x RocketIO™ to front panel 10Gbps CX4 connector, option to AMC ports 17-20

DSPs: Three 1GHz multicore TMS320TCI6487 DSPs. TCI6488 option.

Each DSP has:

- 128Mbytes x16 DDR2-667 SDRAM
- Two 1x SRIO ports to switch
- One Gigabit Ethernet port to switch
- Four Antenna Interface Links
- DSP boot options include FLASH, SRIO and Ethernet

Debug: DSP or FPGA JTAG debug via Breakout Board (AMC-BB)

Antenna Interface: 2 SFP sockets for optical CPRI RE/REC and OBSAI RP3-01 compliant antenna interface links, connected to FPGA RocketIO. Also usable for other optical links such as SRIO, GigE or Aurora. Data rate up to 4Gbps per link.

Clock Synchronisation: Low-jitter VCXO based PLL, digitally controlled from the FPGA. Allows clock synchronisation and distribution from an external 30.72 MHz or 1PPS GPS clock via AMC backplane, front panel (option) or SFP SERDES. IEEE1588 is also possible.

Serial RapidIO: 10Gbps 4x infrastructure using Tundra Tsi578™ switch:

- AMC.4 compliant 10Gbps 4x connections to AMC ports 4-7 and 8-11
- Dedicated 10Gbps 4x link to FPGA
- Optional Front Panel 10Gbps 4x link

Ethernet: Gigabit Ethernet infrastructure using Broadcom BCM5389™ switch:

- AMC.2 (1000BASE-BX) compliant connections to AMC Ports 0 & 1
- Full-duplex 1Gbps links

IPMI: ATMega128 IPMI controller:

- AMC.0 IPMB_L interface
- FRU EEPROM data
- Power & reset control, health monitoring

Form Factor: Advanced Mezzanine Card

- AMC.0 Rev 2.0 compliant
- Full-size, single-width
- AMC.2 GigE and AMC.4 4x SRIO
- Hot swap support

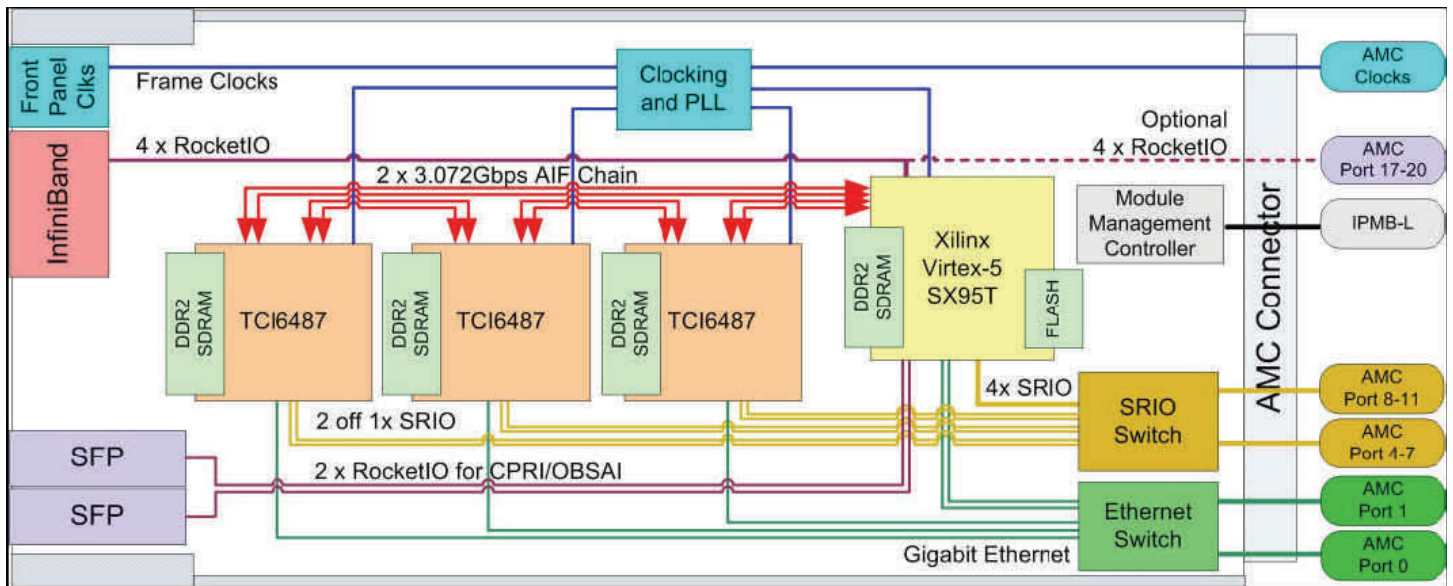


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ENVIRONMENTAL/EMC/SAFETY

- Operating temperature: 0-40 C ambient
- Power consumption: up to 48W max, dependent on SFPs used and FPGA load
- Designed for NEBS and ETSI compliance when used in appropriate chassis
- 2004/108/EC and FCC EMC compliant
- 2002/95/EC RoHS, 2002/96/EC WEEE and 2006/95/EC Low Voltage Directive compliant

SOFTWARE SPECIFICATIONS

FPGA: to demonstrate configuration and functionality; Xilinx ISE and EDK project
MicroBlaze Board Support Library (BSL): support for board setup and interfaces, self test and FLASH update
MMC: full management suite based on PigeonPoint BMR software
DSP Board Support

Ordering:

VRM-AMC-3C87F: High performance signal processing AMC card for wireless baseband solutions including WiMAX and LTE.