



V Rose Microsystems, Inc.

www.vrosemicrosystems.com

VRM-AMC-V5F

Product Data Sheet

Overview:

The VRM-AMC-V5F is a single width, mid-size Advanced Mezzanine Card. It is aimed at the latest wireless baseband applications but also very suitable for any high performance FPGA processing application, especially where optical interfacing or SRIO support is required.

A Xilinx Virtex-5 SX95T FPGA provides the main processing. This configures and boots from FLASH on reset, using one of 4 selectable configuration images which are customer programmable and can be updated over Ethernet. The FPGA is fully customer configurable. The FPGA build normally contains a Microblaze processor for basic board configuration and control, and a full example FPGA build and Microblaze Board Support Package is provided.

The dual SFP sockets for optical interfaces to the FPGA are key features of the VRM-AMC-V5F. These are typically used for CPRI or OBSAI interfaces, although many other options are possible. Linked to this interface is a highly flexible, low jitter programmable PLL circuit, allowing

a wide range of wireless synchronization options including a low cost 1 PPS GPS clock

A range of build options are available, and further customization is possible in volume, to enable the best technical and commercial fit to a



Features:

FPGA: Xilinx Virtex-5 FPGA. Standard configuration is SX95T-2, options include LX110T, LX155T, FX100T. With:

- 2 independent banks of 128Mbytes x 16 DDR2-600 SDRAM
- 128Mbytes of parallel FLASH
- 10Gbps 4x SRIO
- 2 Full-duplex Gigabit Ethernet ports
- 4x RocketIO to front panel 10Gbps CX4 connector, option to AMC ports 17-20

Antenna Interface: 2 SFP sockets for optical CPRI RE/REC and OBSAI RP3-01 compliant antenna interface links, connected to FPGA RocketIO. Also usable for other optical links such as SRIO, GigE or Aurora, Data rate up to 4 Gbps per link.

Clock Synchronization: Low-jitter VCXO based PLL, digitally controlled from the FPGA. Allows clock synchronization and distribution from an external 30.72 MHz or 1PPS GPS clock via AMC backplane, front panel (option) or SFP SERDES. IEEE1588 is also possible.

Serial RapidIO: 10Gbps 4x infrastructure using Tundra Tsi578 switch:

- AMC.4 Compliant 10Gbps 4x connections to AMC ports 4-7 and 8-11
- Dedicated 10Gbps 4x link to FPGA
- Optional Front Panel 10Gbps 4x SRIO link using CX4 connector

Ethernet: Gigabit Ethernet infrastructure using Broadcom BCM5389 switch:

- AMC.2 (1000BASE-BX) compliant connections to AMC Ports 0 & 1
- Full-duplex 1Gbps links

IPMI: ATmega128 IPMI controller:

- AMC.0 IPMB_L interface
- FRU EEPROM data
- Power and reset control
- Real-Time health monitoring

Form Factor: Advanced Mezzanine Card

- AMC.0 Rev 2.0 compliant
- Mid-size, single-width; also available as full-size on request
- For AdvancedTCA and MicroTCA
- AMC.2 GigE and AMC.4 4x SRIO
- Hot swap support



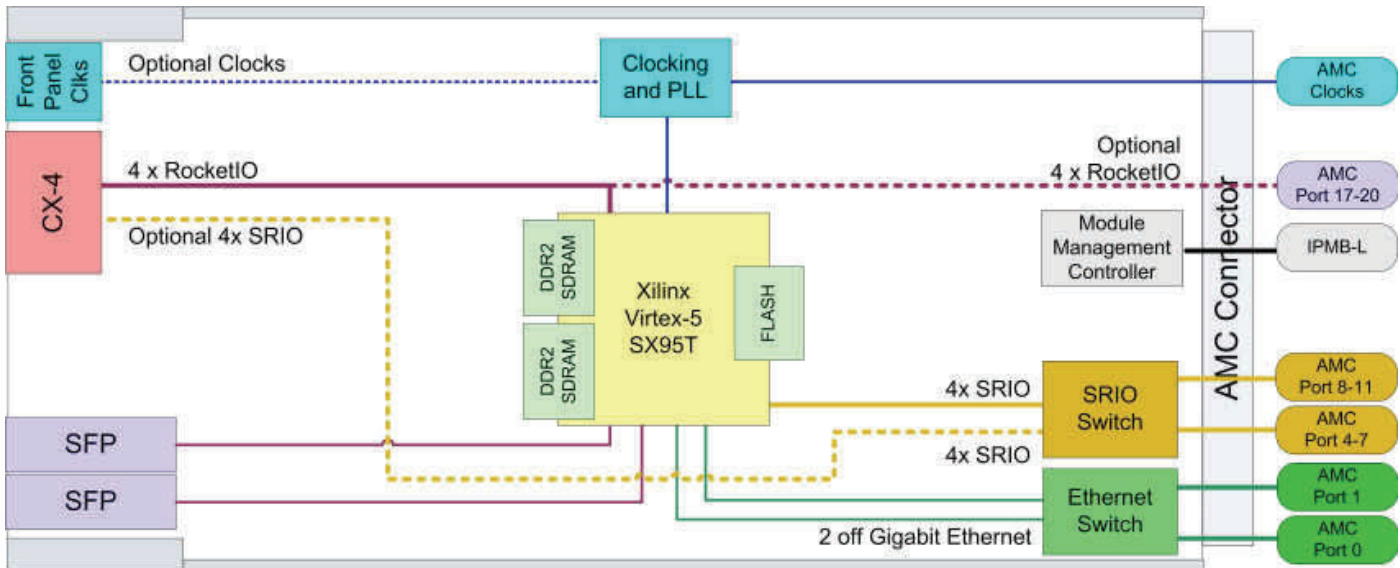
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Block Diagram:



Ordering:

VRM-AMC-V5F: Single width mid-size Advanced Mezzanine Card