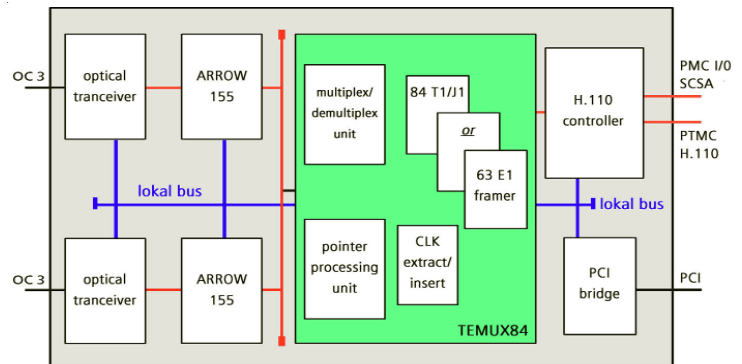


Overview:

The **VRM-PMC-STM1-X-X** is a telecommunications interface board in PMC form factor. The **VRM-PMC-STM1-X-X** is targeted at telecom applications dealing with SDH (Synchronous Digital Hierarchy), such as SS7, ISDN or 3G/3.5G mobile applications in optical OC-3/STM-1 and SONET environments.

Being equipped with an add/drop multiplexer/demultiplexer chipset the **VRM-PMC-STM1-X-X** is an ideal single board platform to interface between the frame oriented STM-1/SDH networks and classic TDM (Time Division Multiplex) standards as E1/T1/J1. Possible applications are add/drop multiplexer or terminal multiplexer.



Features:

PCI Interface: P1386.1 Draft 2.0 compatible PMC module that can be plugged onto any VME, cPCI or other carrier board offering a PMC extension slot. The PCI-to-local-bus Bridge directly interconnects the PCI bus to the local bus and the onboard devices. The VRM-PMC-STM1-X-X is PCI Rev 2.2 compatible (32 bit).

Optical Interface: The two optical 155Mbps OC-3/STM-1 line interfaces are available on two standard OC-3 SDH/STM-1 connectors at the front panel. The transceivers are available for single or multi-mode fibre access. Each of the transceivers is connected to a PMC-Sierra ARROW 155 framer, both framers being connected to each other supporting the Automatic Protection Switching (APS).

VT/TU Access: The two ARROW155 framers are connected to the TEMUX84 of PMC-Sierra, an add/drop Multiplexer/demultiplexer chip. Since the chip does the complete SDH pointer processing it is capable of accessing STS-1 SPEs (Synchronous Payload Envelopes), TUG3 tributary unit groups within VC4 container as well as in VC3 virtual containers and thus to extract/insert any of the 84 T1/J1 or 63 E1 streams including the respective clocking information contained in a single STM-1 SDH frame. Supported mappings are VT1.5/VT-2 to STS-1 SPE, TU-11/TU-12 to STM-1/VC3 or TUG3 to STM-1/VC4. The chip supports the M13 and G.747 multiplexing.

T1/J1/E1 Access: The multiplexer/demultiplexer function block of the TEMUX84 interfaces to internal 84 T1/J1 framers or 63 E1 timesliced framers, each having individual Rx/Tx, CLK and SYNC signals. For T1 the framing standards SF,SLC-96 and ESF, for E1 G.704 and G.706 (CRC-4 multiframe), for J1 the TTC JT-G.704 as well CRC-6 calculation are supported. The chip also provides full jitter attenuation.

H.110 interfaces: The T1/J1/E1 framers interface to the onboard H.110 controller, the Zarlink MT90866. The H.110 controller allows flexible 64kbps timeslot routing between the various T1/J1/E1 streams as well as the selection of one of the T1/J1/E1 clocks as the master clock for the TDM backplane bus. Thus it is possible to distribute all 84 T1/J1 or 63 E1 streams jitter-free and synchronised via the backplane.

Backplane TDM Access: The onboard H.110 bus controller offers access to the backplane TDM bus supporting full the H.110 bus (PTMC) or the SC Bus subset on the PMC multi-purpose I/O connectors.

PCI Interface and Compliance: PCI Rev 2.2, 33MHz/32bit

H.110 Bus (and subsets thereof): H.110 (PTMC) and SCSA subset

Networking: two OC3 SDH/STM1 optical fibre on standard connector at front panel (SC duplex single or multimode transceiver)

Indicator LEDs: 4 software programmable LEDs at the front panel

Operating System Support: OK-1, VxWorks, LINUX

Power Consumption: 3.3V 2.2A (max), to be determined

Environmental: Temperature (operating): 0C to +60C with forced air cooling. Temperature (storage): -40C to +85C. Relative Humidity: 10% to 90% at +55C (non-condensing)

Standard Compliance: P1386 and P1386.1/Draft 2.0

Applications: high density multiplexers, multi-service switches, edge routers and digital modems, Frame Relay switches and access devices, SONET/SDH add drop and terminal multiplexers, optical access equipment, digital access cross-connect systems.

Ordering options:

Single mode or Multi mode / Single TEMUX84 or dual TEMUX84